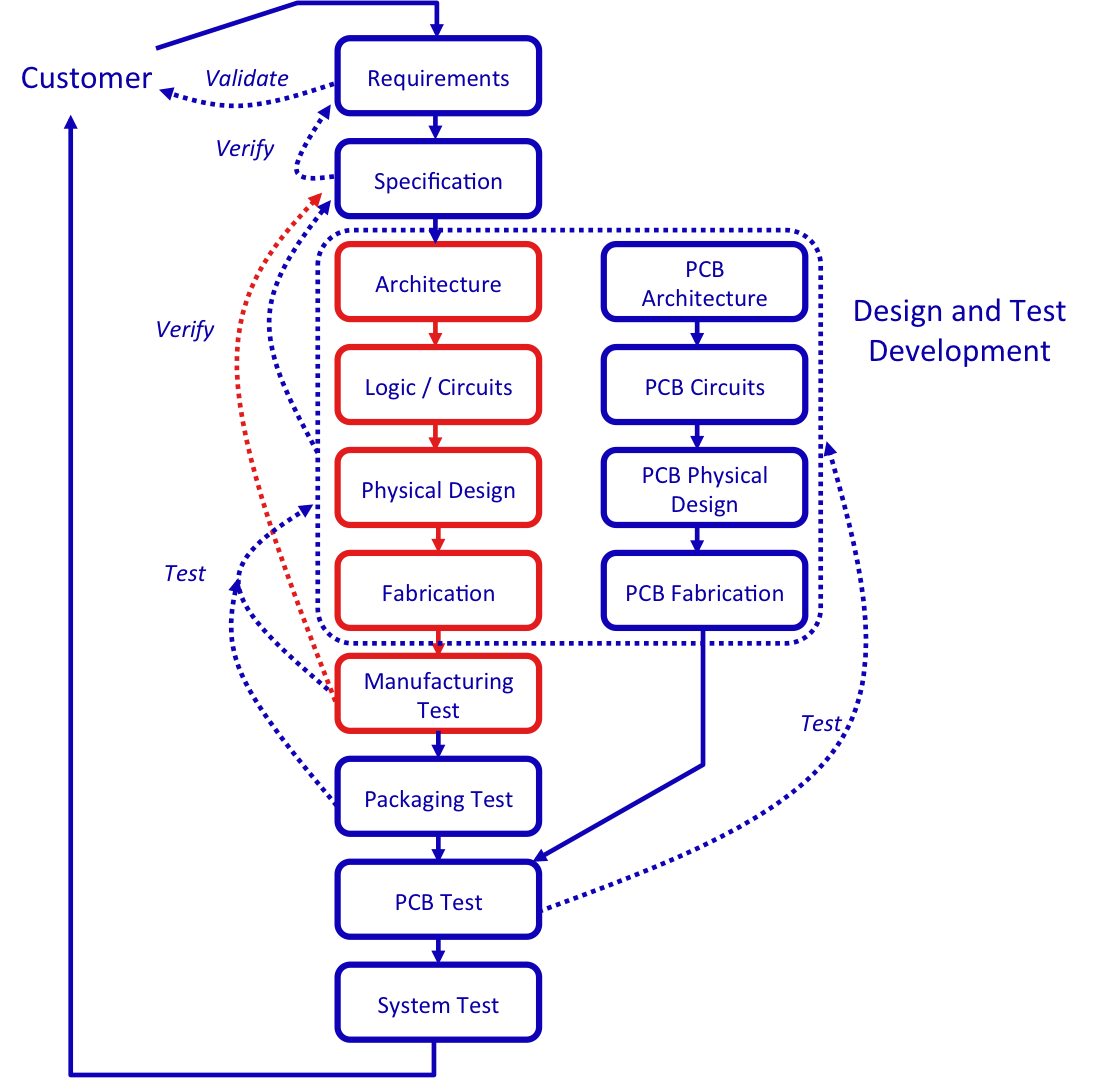
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ECE 7502

Project Proposal

**Context**



**Figure 1. This is the general flow for the IC verification and test process. Highlighted in red are the portions of the test flow that I am focusing on in this project.**

As ICs continue to scale, power consumption becomes an increasingly important concern, making sub-threshold (sub-VT) an attractive route for many ultra low power (ULP) applications.  Many such applications utilize energy harvesting, a mechanism by which energy already present in the environment powers a device. Such energy may occur naturally (e.g. solar energy, body heat) or due to emissions from existing technologies (e.g. electromagnetic energy). Because the energy is already present, this is essentially free energy, making energy harvesting an extremely popular avenue for designers with ULP applications.

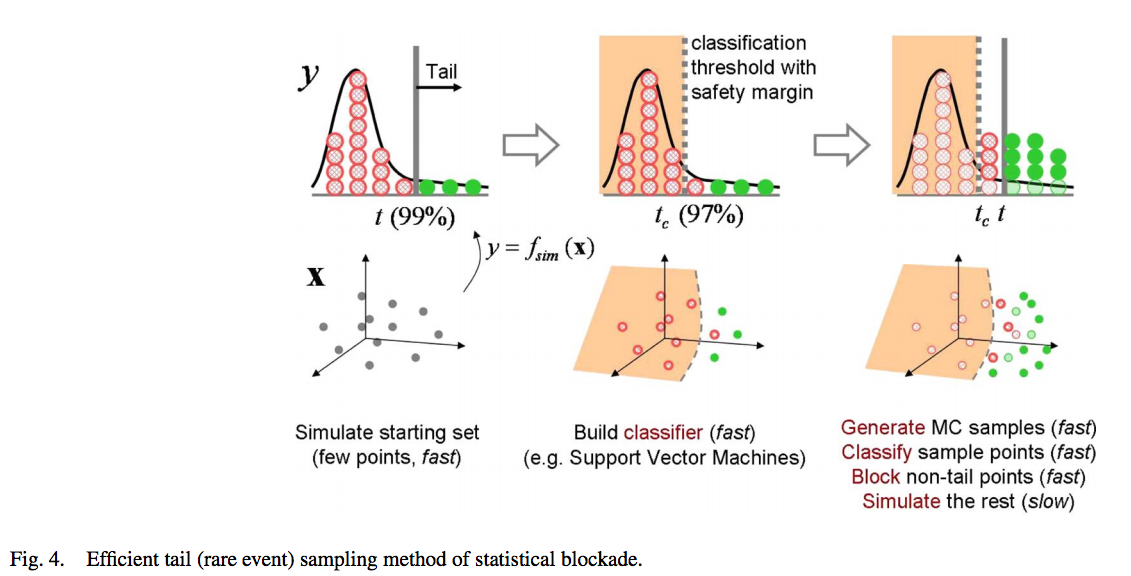
A major roadblock to usability of such applications lies in increased sensitivity to variations both at near- (NVT) and sub-VT. Therefore, thorough and accurate assessment of variation robustness pre-Si is vital. Additionally, many energy-harvesting applications have to be able to withstand a wide range of extreme temperatures since they are operating in outdoor environments. This makes adaptability to a variety of temperatures an important characteristic of such designs. Monte Carlo (MC) simulations are often run in order to simulate variations at a variety of process corners and temperatures.

Moreover, determination of test coverage post-Si is still a difficult problem. The question of the most effective and efficient way to test a design is still an open problem. This problem may be approached differently based on the application for which the design is used as well as on the problems anticipated by pre-Si testing. Therefore, with thorough simulation one might be able to improve the required time for test by anticipating post-Si problems and testing for those first. Because in sub-VT many of the issues are variation related (this has also begun to ring true for many super-threshold (super-VT) designs due to the increasingly small scale at which devices are manufactured), many issues can be anticipated with MC analysis. The question arises, how we can use MC simulations at a variety of process corners and temperatures to most effectively test our circuit for variations post-Si. This project focuses on the Design and Test Development portion of the test flow with some discussion of Manufacturing Test as illustrated by Figure 1.

**Previous Work**

Much of the previous work on this subject has been with respect to analog ICs. For example, [4] seeks to address the issue of fault coverage in analog ICs. The authors motivate this problem by explaining that test cost for analog ICs is much higher than for digital ICs. This paper is one of a collection seeking to minimize test cost while maintaining test accuracy. They explain that one can use MC simulation to determine probabilistic fault coverage. But Defining fault models for analog ICs becomes computationally intensive because generating the tail cases in a MC can be very time consuming. Similarly, [3] addresses the high test cost associated with a brute force testing method, that is, testing all possible paths for which specifications were provided.

**[1] Singhee, Amith, and Rob A. Rutenbar**



[1] and [2] present a technique called Statistical Blockade (SB). This technique reduces the amount of time needed to simulate with MC by isolating the cases in the tail of the distribution. SB does this by identifying a classification threshold and setting an indicator variable. This is the technique used in [4] and [5] to achieve the desired results, as well.

**Problem Statement**

My project seeks to answer two main questions. First, is there any correlation between process corners and temperature? For example, at lower temperatures, could the FF corner behave more like the TT corner at room temperature? Could the SS corner at higher temperatures behave like the TT corner at room temperature? In general, can we achieve the same results as ideal (TT at room temperature) simply by varying the temperature at which the design operates given a particular process corner? Second, given what we find, how does this influence the test coverage needed to determine the process corner at which the design is ultimately fabricated? How do we determine what needs to be tested and how we test it?

**Approach**

My approach will be to run MC simulations at different temperatures between -55°C and 125°C (military standard for device robustness to temperature) for each of the process corners (SF, FS, SS, FF, TT) at a variety of supply voltages. I will run the following simulations:

* Static simulations will be:
  + Static noise margins (SNMs) from VTCs of 2-to-1 mux, 2-input NAND/NOR, and inverter gates
  + Determine minVDD (where SNMs no longer exist)
* Transient simulations will be:
  + Frequencies of ring oscillators (ROs) of different sizes (9, 25, and 49 device) composed of 2-to-1 mux, 2-input NAND/NOR, and inverter gates
  + Determine minVDD (where ROs no longer ring)

The next component of my project will be to determine how my findings from the MC analyses influence the test coverage I need. In order to do this I would like to see if I can understand how to apply SB to the MC simulations I run and see if I can apply it to testing post-Si as well.

**Results**

I expect to see trade-offs emerge between extreme temperatures and worst-case process corners that allow the design to function as well as the best case TT 27°C. My deliverables will include the plots from simulating MC at different process corners, temperatures, and supply voltages as well as an analysis of how my findings influence the kind of test coverage I need.

**Milestones**

3/3/15 – Project Report 1

* Run MC simulations at TT, FF, SS at -55°C, 27°C, 125°C for VDD=50mV-1V
  + SNMs for inverter, 2-to-1 mux, and 2-input NAND/NOR gates
  + Transient analysis on 9, 25, and 49 device ROs
  + minVDD analysis—at what voltage do the ROs fail transiently and individual devices fail statically

3/24/15 – Project Report 2

* Run MC simulations at FS, SF at -55°C, 27°C, 125°C for VDD=50mV-1V
  + SNMs for inverter, 2-to-1 mux, and 2-input NAND/NOR gates
  + Transient analysis on 9, 25, and 49 device ROs
  + minVDD analysis—at what voltage do the ROs fail transiently and individual devices fail statically

4/16/15 – Final Project Report

* Compare simulations and identify trade-offs
* Discussion of what my findings tell us about the test coverage needed post-Si

**References**

[1] Singhee, Amith, and Rob A. Rutenbar. "Statistical blockade: very fast statistical simulation and modeling of rare circuit events and its application to memory design." *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 28.8 (2009): 1176-1189.

[2] Singhee, Amith, et al. "Recursive statistical blockade: An enhanced technique for rare event simulation with application to SRAM circuit design." *VLSI Design, 2008. VLSID 2008. 21st International Conference on*. IEEE, 2008.

[3] Stratigopoulos, Haralampos-G., and Stephen Sunter. "Efficient Monte Carlo-based analog parametric fault modelling." *VLSI Test Symposium (VTS), 2014 IEEE 32nd*. IEEE, 2014.

[4] Stratigopoulos, H., and Stephen Sunter. "Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics." *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 33.12 (2014): 1977-1990.